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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
ISAAC, STANETTA D	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 12/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/885,761	KUWAZAWA, KAZUNOBU	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 21-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 21-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 November 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Lynne A. Gurley

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed on 9/27/04. Currently, claims 1-9 and 21-29 are pending.

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 26 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is indefinite whether the "sidewall protection layer" in claim 26, is an additional layer to the extension control layer and the sidewall mask layer. For examination purposes, on the merits, the Examiner will assume that that the "sidewall protection layer" is the "extension control layer".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-9, and 21-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al., US Patent 4,855,247 in view Oishi et al. US Patent 6,335,252.

Ma discloses the semiconductor method substantially as claimed. See figures 1(a)-3(c), and corresponding text, where Ma shows, pertaining to claim 1, a method for manufacturing a semiconductor device, the method comprising: (a) forming a gate dielectric layer **12** over a semiconductor substrate **10** (figure 2(a); col. 6, lines 8-15); (b) forming a gate electrode **14** over the gate dielectric layer (figure 2(a); col. 6, lines 8-15); (c) forming a dielectric layer **20** over the substrate (figure 2(a); col. 6, lines 1-15); (d) forming a mask layer **23** (figure 1(a)) over the dielectric layer (figure 2(a); col. 6, lines 1-7 and lines 16-22); (e) anisotropically etching the mask layer to form a sidewall mask layer **24** on sides of the gate electrode over the dielectric layer (figure 2(a); col. 6, lines 1-7 and lines 16-23 ***Note***: as stated in col. 4, lines 54-62, "that a directional silicon nitride etch is performed", is well known in the art, that directional etching is anisotropic); (f) isotropically etching the dielectric layer using the sidewall mask layer as a mask to form an extension control layer and a sidewall protection layer on sides of the gate dielectric layer (figure 2(b); col. 6, lines 20-26, ***Note***: that wet-etching is done isotropically. *Stanley Wolf and Richard N. Tauber, Silicon Processing For The VLSI Era, Vol. I, Lattice Press, 1986, pages 522-535*); and (g) ion-implanting an impurity in the semiconductor substrate, wherein the ion-

implanting includes implanting an impurity through the extension control layer into the semiconductor substrate and the implanting also includes implanting an impurity directly into the semiconductor substrate in a region adjacent to the extension control layer; wherein an extension region **32** is formed in the semiconductor substrate below the extension control layer during the ion-implanting, and source and drain regions **34** are formed in the semiconductor substrate adjacent to the extension region (figure 2(c); col. 6, lines 56-67; col. 7, lines 1-25); In addition, Ma shows, pertaining to claim 2, wherein the step (f) further includes the step of forming a sidewall protection layer on sidewalls of the gate electrode (figure 2(b); col. 6, lines 20-26). Also, Ma shows, pertaining to claim 3, further including removing the sidewall mask layer after the isotropically etching the dielectric layer and prior to the ion-implanting (figure 2(c); col. 6, lines 49-65). Also, Ma shows, pertaining to claim 6, wherein the extension control layer formed from a material comprising silicon dioxide (col. 6, lines 8-15). Ma shows, pertaining to claim 7, wherein the sidewall mask layer is formed from a material comprising silicon nitride (col. 6, lines 8-15). In addition, Ma shows, pertaining to claim 8, wherein the extension control layer has a thickness of 5-50 nm (col. 6, lines 16-30). Also, Ma shows, pertaining to claim 9, wherein the sidewall mask layer is formed to a thickness of 30-200 nm (col. 4, lines 45-54). Finally, Ma teaches, pertaining to claim 27, wherein the ion-implanting is carried out in a single ion implanting operation (figure 2(c); col.6, lines 57-67; col. 7, lines 1-25).

Ma shows, pertaining to claim 21, a method for manufacturing a semiconductor device including extension regions and source/drain regions formed using a single ion-implantation step, the method comprising: forming a gate dielectric layer **12** over a semiconductor substrate **10** (figure 2(a); col. 6, lines 8-15); forming a gate electrode **14** over the gate dielectric layer

(figure 2(a); col. 6, lines 8-15); forming extension control structures **22/30** over a portion of the semiconductor substrate next to the gate dielectric layer by forming a dielectric layer on the semiconductor substrate, forming a mask layer on the dielectric layer, anisotropically etching the mask layer to form a sidewall mask layer (figure 2(a); col. 6, lines 1-7 and lines 16-23 ***Note***: as stated in col. 4, lines 54-62, "that a directional silicon nitride etch is performed". It is well known in the art, that directional etching is anisotropic), and isotropically etching the dielectric layer after forming the sidewall mask layer (figure 2(b); col. 6, lines 20-26, ***Note***: that wet-etching is done isotropically. *Stanley Wolf and Richard N. Tauber, Silicon Processing For The VLSI Era, Vol. I, Lattice Press, 1986, pages 522-535*); and a single ion-implanting operation that forms extension regions in the semiconductor substrate under the extension control structures and forms source and drain regions in the semiconductor substrate adjacent to the extension regions, wherein the extension regions have a depth that is less than that of the source/drain regions and wherein the ion-implanting operation includes implanting through the extension control structures to form the extension regions, and the ion-implanting operation includes implanting directly into the semiconductor substrate adjacent to the extension control structures to form the source drain regions at the same time that the extension regions are being formed (figure 2(c); col.6, lines 57-67; col. 7, lines 1-25). In addition, Ma shows, pertaining to claim 22, further comprising forming sidewall protection structures on sidewalls of the gate electrode during the isotropically etching the dielectric layer (figure 2(b); col. 6, lines 20-26). Also, Ma shows, pertaining claim 23, further comprising removing the sidewall mask layer prior to the ion-implanting (figure 2(c); col. 6, lines 49-65). Ma shows, pertaining to claim 25, wherein the extension control layer is formed from silicon oxide (col. 6, lines 8-15).

Ma shows, pertaining to claim 28, a method for manufacturing a semiconductor device, comprising: forming a gate dielectric layer over a semiconductor substrate; forming a gate electrode over the gate dielectric layer (figure 2(a); col. 6, lines 8-15); forming a dielectric layer over the substrate (figure 2(a); col. 6, lines 1-15); forming a mask layer over the dielectric layer (figure 2(a); col. 6, lines 1-7 and lines 16-22); etching the mask layer as mask to form a sidewall mask layer on sides of the gate electrode; etching the dielectric layer using the sidewall mask layer as a mask to form extension control layer and a sidewall protection layer on the sides of the gate dielectric layer (figure 2(a); col. 6, lines 1-7 and lines 16-23); and forming an extension region in the semiconductor substrate by ion-implanting impurity ions into the substrate through the extension control layer (figure 2(c); col. 6, lines 49-65); forming source and drain regions in the semiconductor substrate by ion-implanting impurity ions into the substrate (figure 2(c); col. 6, lines 49-65); In addition, Ma shows, pertaining to claim 29,further comprising forming the extension region and the source drain regions during the same ion-implanting operation (figure 2(c); col.6, lines 57-67; col. 7, lines 1-25).

However, Ma fails to show, pertaining to claims 1, 21 and 28, (h) forming a metal layer over the semiconductor substrate and heating the metal layer to form a silicide on upper portions of the source and drain regions and on an upper portion of the gate electrode, wherein the extension control layer above the extension region inhibits the formation of a silicide on the extension control layer during the heating. In addition, Ma fails to show, pertaining to claims 4, 5, 24 and 26, wherein the extension control layer is formed from a material comprising silicon nitride and wherein the sidewall mask layer is formed from a material comprising silicon oxide.

Oishi teaches, in figures 1-7, and corresponding text, a similar method of manufacturing a semiconductor device, the step of h) forming a metal layer over the semiconductor substrate and heating the metal layer to form a silicide on upper portions of the source and drain regions and on an upper portion of the gate electrode, wherein the extension control layer above the extension region inhibits the formation of a silicide on the extension control layer during the heating (col. 7, lines 42-57). In addition, Oishi teaches, wherein the extension control layer is formed from a material comprising silicon nitride and wherein the sidewall mask layer is formed from a material comprising silicon oxide (col. 6, lines 11-17).

It would have been obvious to one of ordinary skill in the art to incorporate, the step of (h) forming a metal layer over the semiconductor substrate and heating the metal layer to form a silicide on upper portions of the source and drain regions and on an upper portion of the gate electrode, wherein the extension control layer above the extension region inhibits the formation of a silicide on the extension control layer during the heating, and the step of wherein the extension control layer is formed from a material comprising silicon nitride and wherein the sidewall mask layer is formed from a material comprising silicon oxide, pertaining to claims 1, 4, 5, 21, 24 and 28, in the method of Ma, according to the teachings of Oishi, with the motivation that, Oishi teaches, in a similar structure,with an extension region, the self-aligned silicide structure (salicide), including forming a silicide over the gate, source and drain regions, that a silicide may be formed after the extension regions are formed, for the purpose of reducing the resistance between the source/drain regions. In general, silicides are well known for their ability to lower resistivities, and to join to contact metals, etc. Note that no silicide is formed on the extension control layer, therefore, it would have been obvious to one of ordinary skill in the art

that the extension control layer would be used to inhibit the formation of a silicide on the extension control layer during the heating, for the purpose of preventing silicide formation on the lightly doped regions.

It would have been obvious to one of ordinary skill in the art to incorporate, the extension control layer and the sidewall mask layer being formed of the materials, silicon nitride and silicon oxide, respectively, pertaining to claims 4, 5, 24 and 26, the method of Ma, according to both the teachings of Ma in view of Oishi, with the motivation that, both Ma and Oishi, teach that the implied extension control layers and sidewall mask layers are made by either silicon nitride or silicon oxide respectively, and that by using conventional etching methods both layers can be selectively etched anisotropically or isotropically etched with respect to each other. For example, Ma teaches, that the implied sidewall mask layer is made of a silicon nitride material and, Oishi teaches, that the implied sidewall mask layer is made of a silicon oxide material, both materials may be etched either anisotropically or isotropically. As a result, the materials used prove to be interchangeable since the end results are identical to the formation of the extension control layer and the sidewall mask layer in either Ma or Oishi.

Response to Arguments

Applicant's arguments with respect to claims 1-9 and 21-26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on 571-272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
December 2, 2004

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